EE / CPRE / SE 491 - sdmay20-38
iFPGA - Intermittent Intelligent FPGA Platform
Week7 Report

10/14/19 - 10/20/19
Client: Henry Duwe
Faculty Advisor: Henry Duwe

Team Members:

Jake Tener - Team member, SW focus
Jake Meiss - Team member, HW focus
Andrew Vogler - Team member
Zixuan Guo - Team member
Justin Sung - Team member

Weekly Summary

This week, we continue to do the FPGA related search and the sound classification intro. For FPGA related, based the FPGA board we have chosen, we use Libero to get the power that components need and based on this data to use the corresponding formula to consume its power consumption. For the sound classification intro, Jake Tener have built a prototype of sound classification based on Python.

Past Week Accomplishments

- FPGA HW synthesis - Justin Sung, Andrew Vogler
    - Created simple adder components to synthesize on various sizes of IGLOO nano and the IGLOO+ to determine how much computational power is utilizable on the chips.
    - Synthesis results recorded on the spreadsheet, the largest IGLOO nano is most promising so far.
- Platform/Harvester power analysis - Jake Meiss, Zixuan Guo
    - Formulated a system in order to calculate specifications such as Power consumption and output voltage, capacitance sizing, and charging/discharging times
    - Researched benefits and problems with different sizes and types of capacitors that would fulfill necessary specifications
    - Began taking measurements in the lab for RF energy harvested under different conditions
    - Research on the current and voltage change when the FPGA is on boosting and off situation.
- Audio classification research - Jake Tener
    - Build a prototype of a sound classification program based on the Python

- Machine Learning is used in its program. Program can learn the sound type by itself and improve its accuracy on prediction.
- Training the program based on a large sound database.

Pending Issues

- To sketch an IP block and its inside data flow.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Jake Tener	Programming the sound classification	8	55
Jake Meiss	Platform/Harvester power analysis	8	51
Andrew Vogler	FPGA HW synthesis	8	51
Zixuan Guo	Power requirement analysis	8	51
Justin Sung	FPGA HW synthesis	8	51

Plans for Coming Week

- Power Calculations on the Igloo Nano AGLN250 (Jake Meiss)
  - Spreadsheet / Document entailing calculations
  - Estimated amount of capacitance in the array for running the FPGA
- Researching and Placing IP Blocks in Libero (Andrew and Zixuan)
  - Libero schema created
- Looking into loading Linux kernel onto the FPGA for running python code
  - Document entailing research
- Diagram Flow of Sound to classification
  - Flow from .wav file to classification
- Test sample sounds
  - Classification of random custom sounds to see how the model reacts